REMARKS

This Amendment is responsive to the Office Action dated July 30, 2003. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination is respectfully requested.

At paragraphs 2-3 of the Office Action, the Examiner objected to claim 17 as being a duplicate of claim 16. Claim 17 has been cancelled herein.

At paragraphs 4-5 of the Office Action, the Examiner rejected claims 1 and 5 under 35 U.S.C. 102, as being anticipated by the IBM Technical Disclosure Bulletin dated August 1991, and entitled "Tagged Inter Processor Communication Bus for Multiprocessor Systems" ("Tagged" hereafter). Applicants respectfully traverse this rejection.

Tagged discloses a low-latency inter processor communication (IPC) bus for supporting communications between multiple processors and other devices. The Tagged IPC bus uses a tagging scheme to identify requests, and supports simultaneous processor requests and memory replies during the same bus cycle. The system described in Tagged includes support for slave devices (non-processor devices), which operate in response to read cycles by requesting the bus for returning error correction code (ECC), data, and data identifier values.

Nowhere in Tagged is there disclosed or suggested any system or method for transferring data that includes ***a master request bus and a slave request bus***, and that initiates an operation utilizing a protocol when a master request and an arbiter grant is received ***from the master request bus***, and wherein the protocol enables transfer of data between computer hardware operating according to different protocols, as in the present claims 1 and 5. While Tagged describes slave devices that respond to bus read cycles by providing data over the bus,

Tagged includes no hint or suggestion of even the desirability of having a master bus and a slave bus, as in the presently claimed invention set forth in claims 1 and 5. Instead, Tagged only describes a data bus (D-bus) and an address bus (A-bus). The D-bus of Tagged includes data lines, while the A-bus includes address lines, as is common in bus design. The D-bus and A-bus of Tagged do not have a structure or behavior that could be considered equivalent to the split master bus/slave bus design as set forth the present claims 1 and 5, which advantageously allows the use of separate master and slave bus arbiters for the master and slave bus portions, thus improving overall performance of the system.

For the reasons above, Applicants respectfully urge that the disclosure of Tagged does not disclose or suggest all the features of the present independent claims 1 and 5. Tagged accordingly does not anticipate the present independent claims 1 and 5 under 35 U.S.C. 102. Reconsideration is respectfully requested.

At paragraph 6 the Examiner indicated that claims 2-4, 6-16 and 18 contain allowable subject matter. Claims 2 and 6 have accordingly been re-written in independent format, and claims 3-4, 7-16 and 18 depend therefrom.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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